Improved Interleaved Boost Converter with Soft-Switching: Analysis and Experimental Validation

Madhuchandra Popuri
School of Electrical Engineering, Kalinga Institute of Industrial Technology, India
mcpopuri@gmail.com

Veera Venkata Subrahmanya Kumar Bhajana
School of Electronics Engineering, Kalinga Institute of Industrial Technology, India
bvvs.kumarfet@kiit.ac.in (corresponding author)

Manoj Kumar Maharana
School of Electrical Engineering, Kalinga Institute of Industrial Technology, India
mkmfel@kiit.ac.in

Pravat Biswal
School of Electronics Engineering, Kalinga Institute of Industrial Technology, India
pravat.biswalfet@kiit.ac.in

Bhargav Appasani
School of Electronics Engineering, Kalinga Institute of Industrial Technology, India
bhargav.appasanifet@kiit.ac.in

Mihai Oproescu
Pitesti University Centre, National University of Science and Technology, Romania
mihai.oproescu@upit.ro

Nicu Bizon
Pitesti University Centre, National University of Science and Technology, Romania
nicu.bizon@upit.ro

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ABSTRACT

This paper proposes a novel interleaved boost converter for renewable energy applications. The two-phase interleaved boost converter was improved with lossless passive snubber cells to ensure the Zero Voltage Switching (ZVS) condition. The ZVS condition is contributed by a resonant inductor, a resonant capacitor, and two diodes. The proposed converter was operated in continuous current mode on its primary side. The significant merits of this converter are reduced switching losses, better efficiency, and reduced input current ripples without auxiliary switches. The soft-switching ability of this converter is maintained under both light- and heavy-load conditions. This paper also presents the operating principles and design analysis of the proposed converter. Furthermore, a 50-320V prototype was operated at 250 W to validate the soft-switching operation and theoretical analysis, and the experimental results are presented.

Keywords-DC-DC converter; boost converter; interleaved converter; soft-switching; Zero Voltage Switching (ZVS)

I. INTRODUCTION

In contemporary power conversion systems, boost and Interleaved Boost Converters (IBCs) have gained widespread usage to elevate low-voltage inputs to desired output levels, commonly drawing energy from sources such as wind generator systems [1], DC microgrids [2], and batteries [3]. The tristate interleaved converter design [4] employs auxiliary switches alongside primary switches to alleviate the challenges associated with input current fluctuations and output voltage ripple. However, this converter relies on excessive auxiliary switches and is primarily suited for low-voltage applications.

In response to these limitations, a dual-Coupled Inductor (CI)-based IBC that incorporates a clamping capacitor was proposed in [5]. This innovation serves to reduce voltage stresses and improve overall efficiency. However, it is primarily recommended for low-power applications. Moreover, voltage multiplier cells have been integrated into high-gain converters [6-7] and IBCs [7-8] to achieve improved voltage conversion ratios. In a buck converter, switches are replaced with a resonant switch [9] and IBCs are assisted by a single auxiliary circuit without [10] and with CI [11-13], facilitating soft-switching operation at low power levels. The Zero Voltage Transition (ZVT) condition is achieved when the auxiliary switch operates at twice the converter's switching frequency. Similarly, CIs increase switched capacitor cells, and auxiliary circuits in IBC aim to achieve increased voltage gain and soft-switching operation [14]. However, the auxiliary switches experience elevated current stresses as a result of their higher switching frequency. Similarly, in [15], a large inductor and snubber capacitors were integrated into a conventional IBC to achieve soft-switching, i.e. ZVT condition. Continuing this approach, in [16], an auxiliary switch was used to achieve the ZVT condition. However, these systems typically operate at low voltage and low power levels.

In [17], a different strategy was proposed to achieve soft-switching conditions, involving an IBC with an auxiliary circuit and voltage multiplier cells, which improved overall gain and achieved the ZVT condition. However, this converter primarily functions at very low output power levels. To further improve overall gain, it is necessary to increase the number of windings in current transformers (CIs). Efforts to efficiently recycle leakage energy and operate at high output power levels have led to the utilization of supplementary passive lossless clamp circuits [18] and active clamp circuits [19]. In [20], an increased turns ratio of CIs was implemented to improve voltage gain, coupled with the achievement of Zero Current Switching (ZCS) through a Passive Lossless Clamp Circuit (PLCC) in IBC. This particular converter yielded reduced turn-off losses and an increased overall gain. Similarly, another PLCC-based IBC [21-25] attains ZVS during turn-off in addition to the aforementioned advantages. However, it should be noted that previous IBC designs have exhibited certain disadvantages, including a higher count of active devices, electromagnetic interference (EMI) resulting from increased CIs, complexity in the control circuitry, and operation primarily at low output power levels. To address these limitations comprehensively, this study introduces the novel Soft-Switched Interleaved Boost Converter (SSIBC) equipped with passive auxiliary components: a resonant inductor, a resonant capacitor, and a diode. The proposed converter exhibits several advantages in comparison to the existing IBCs, such as:

- Fewer active and passive devices
- Operates at high power
- Reduces switching losses
- Reduces the voltage stresses in the switching devices.

These advantages make the proposed converter a significant technology with the potential to revolutionize various industries where efficient and high-power conversion is of paramount importance. Figure 1 shows the generalized organization of Renewable Energy Sources (RESs) with IBC, along with loads such as DC microgrids and Electric Vehicles (EVs). Although the source RESs voltage ranges from 12 V to 48 V, the IBC provides a desirable range of 200-500 V for the load.

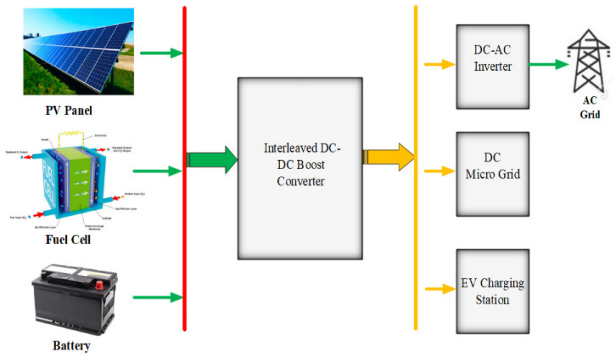

Fig. 1. Generalized organization of RESs with an interleaved boost converter.

II. PROPOSED INTERLEAVED DC-DC CONVERTER

The conventional IBC shown in Figure 2 comprises two inductors (L_1, L_2), two IGBTs (S_1, S_2), and two diodes (D_1, D_2). Figure 3 shows the proposed soft-switching IBC, extended with two passive lossless snubber cells. The passive lossless snubber comprises inductors L_a and L_b, capacitors C_a and C_b, and diodes D_a, D_b, D_c, and D_d. The proposed converter obtains ZVC conditions in their main IGBTs with the help of a passive snubber cell. The following assumptions were considered to describe the steady-state analysis of the proposed converter.

- All IGBTs and passive elements are ideal.
- Parasite circuit components are ignored.
- The size of the output capacitor is large enough to ignore any fluctuations in output voltage.
- Inductors L_1 and L_2 possess significant inductance and exhibit steady currents.

Figure 4 shows the key waveforms, illustrating the operating intervals from t_0 to t_8. Figure 5 shows the equivalent current flow schematics for each interval. The operation of the converter is divided into 8 intervals.

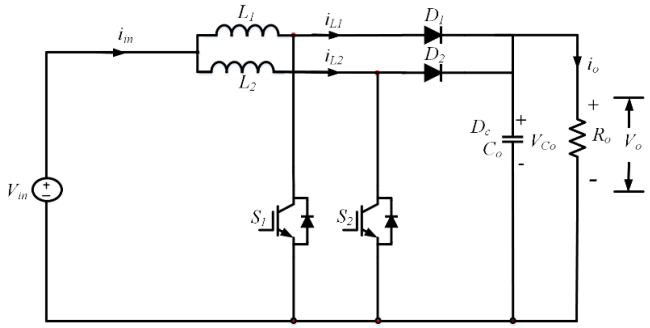

Fig. 2. Conventional interleaved DC-DC converter.

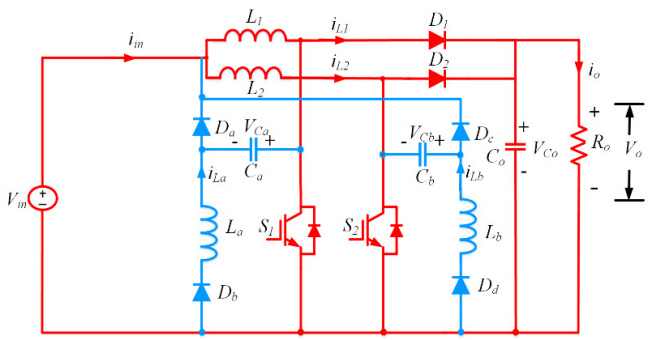

Fig. 3. Proposed interleaved DC-DC converter.

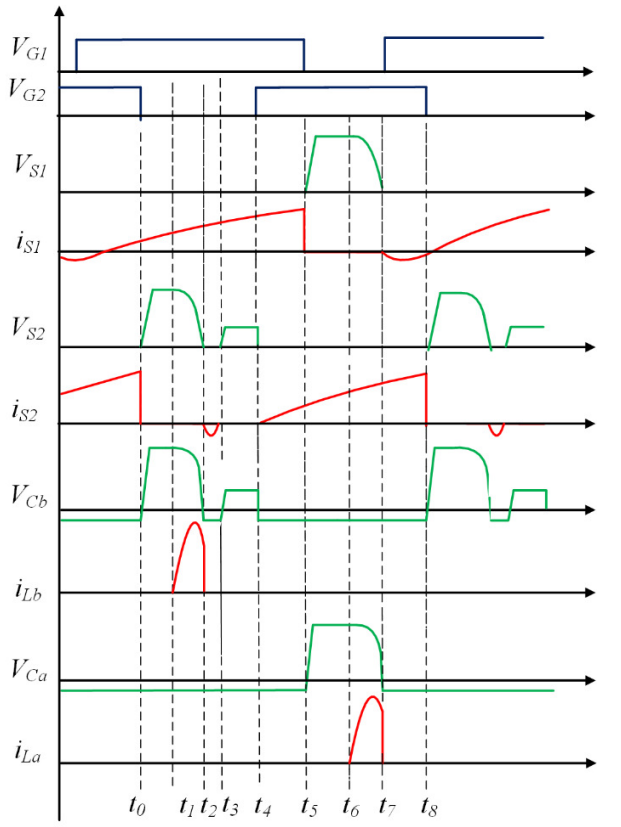

Fig. 4. Key waveforms for the proposed converter.

The steady-state operation of the proposed converter is demonstrated for each interval.

- Interval (t_0-t_1): At t_0, IGBT S_1 is conducting, S_2 is turned off, and hence, output current flows through L_2-D_2. At t_1, the voltage across IGBT S_2 is increased to 2/3 of V_o. The equations of L_1, L_2 and S_2 are:

$$i_{L1}(t) = i_{L1}(t_0) + \frac{1}{L_1}\int_{t_0}^{t_1} V_{in}dt \quad (1)$$

$$i_{L2}(t) = i_{L2}(t_0) - \frac{1}{L_2}\int_{t_0}^{t_1} (V_o - V_{in})dt \quad (2)$$

$$V_{S2}(t) = \frac{1}{C_b}\int_{t_0}^{t_1} (i_{L2}(t) - I_o)dt \quad (3)$$

- Interval (t_1-t_2): At t_1, IGBT S_1 is still conducting and the voltage across IGBT S_2 starts reducing smoothly to reach zero at t_2.

$$i_{L1}(t) = i_{L1}(t_1) + \frac{1}{L_1}\int_{t_1}^{t_2} V_{in}dt \quad (4)$$

$$i_{L2}(t) = i_{L2}(t_1) - \frac{1}{L_2}\int_{t_1}^{t_2} (V_o - V_{in})dt \quad (5)$$

$$V_{S2}(t) = V_o - V_{Cb}(t_1)(1 - cos\ \omega_o\ (t - t_1)) \quad (6)$$

- Interval (t_2-t_3): This is a short interval. At the beginning of the interval, the body diode of S_2 starts conducting and stops at t_3. Hence, the ZVS condition is achieved for S_2. The current expression of IGBT S_2 is as follows:

$$i_{S2}(t) = -(I_o - i_{L2}(t - t_2)) \quad (7)$$

- Interval (t_3-t_4): At t_4, the voltage across IGBT S_2 increases to V_{in} and reaches zero at t_4. The load current continues to flow via L_2-D_2.

$$i_{L1}(t) = i_{L1}(t_3) + \frac{1}{L_1}\int_{t_3}^{t_4} V_{in}dt \quad (8)$$

$$V_{S2}(t) = V_{in} \quad (9)$$

- Interval (t_4-t_5): At the instant t_4, IGBT S_2 is turned on with ZVS condition and S_1 is still conducting. Throughout this interval, the energy is accumulated in inductors L_1 and L_2 via V_{in}-L_1-S_1-L_2-S_2.

$$i_{L1}(t) = i_{L1}(t_4) + \frac{1}{L_1}\int_{t_4}^{t_5} V_{in}dt \quad (10)$$

$$i_{L2}(t) = i_{L2}(t_4) + \frac{1}{L_1}\int_{t_4}^{t_5} V_{in}dt \quad (11)$$

- Interval (t_5-t_6): At t_5, S_1 is turned-off, therefore the output current flows through L_1-D_1-R_o. At t_6, the voltage across S_1 reaches 2/3 of V_o.

$$V_{S1}(t) = \frac{1}{C_a}\int_{t_5}^{t} (i_{L1}(t) - I_o)dt \quad (12)$$

where $t_5 < t < t_6$

$$i_{L2}(t) = i_{L2}(t_5) + \frac{1}{L_1}\int_{t_5}^{t_6} V_{in}dt \quad (13)$$

- Interval (t_6-t_7): Throughout this interval, the voltage across S_1 starts decreasing and reaches zero at t_7.

$$i_{L1}(t) = i_{L1}(t_6) - \frac{1}{L_1}\int_{t_6}^{t_7} (V_o - V_{in})dt \quad (14)$$

$$i_{L2}(t) = i_{L1}(t_6) + \frac{1}{L_2}\int_{t_6}^{t_7} V_{in}dt \quad (15)$$

$$V_{S1}(t) = V_o - V_{Ca}(t_6)(1 - cos\ \omega_o\ (t - t_1)) \quad (16)$$

- Interval (t_7-t_8): At the beginning of this interval, the voltage across S_1 becomes zero and its body diode starts conducting. Therefore, a ZVS condition is obtained. During this interval, S_2 is conducting and energy accumulates in the inductor L_2.

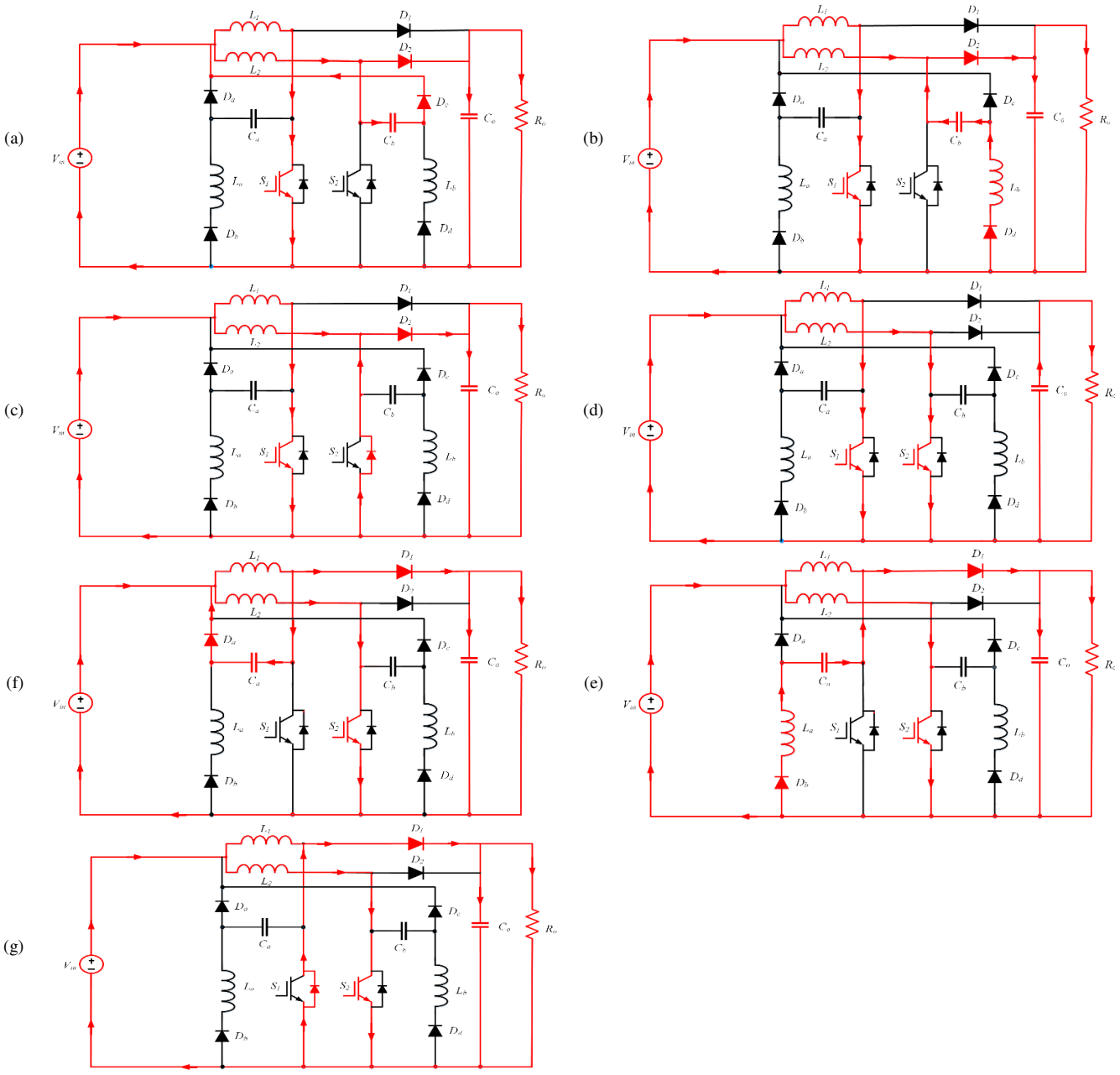

Fig. 5. Equivalent schematics: (a) Intervals (t_0-t_1) and (t_3-t_4), (b) interval (t_1-t_2), (c) interval (t_2-t_3), (d) interval (t_4-t_5), (e) interval (t_5-t_6), (f) interval (t_6-t_7), and (g) interval (t_7-t_8).

III. DESIGN ANALYSIS

The IBC operation was divided into two distinct states to determine the input current ripples of the proposed converter. The first state occurs when S_1 is turned on, while the next is when both S_1 and S_2 are on.

- State 1: In this state, energy gets accumulated in the input inductor L_1 when only S_1 is turned on and the input current gets delivered to output through L_2 since S_2 is turned off. The input current is expressed as follows:

$$\frac{di_{in}}{dt} = \frac{V_{in}}{L} + \frac{V_{in}-V_o}{L} \quad (17)$$

- State 2: In this region, the switching devices S_1 and S_2 are both turned on and energy is accumulated in both the inductors L_1 and L_2. The input current is expressed as follows:

$$\frac{di_{in}}{dt} = \frac{V_{in}}{L} + \frac{V_{in}}{L} \quad (18)$$

The average value of the output voltage V_o is expressed as follows:

$$V_o = \frac{V_{in}}{1-D} \quad (19)$$

$$V_{in} = V_o(1-D) \quad (20)$$

By substituting (19) in (17) and (18), the input current can be expressed as:

$$\frac{di_{in}}{dt} = \frac{V_o}{L}(1-2D) \quad (21)$$

$$\frac{di_{in}}{dt} = \frac{V_o}{L}(2-2D) \quad (22)$$

Input current ripple is defined by (23) for two operating regions; The first is when only one IGBT is turned on ($0 \leq D \leq \frac{1}{2}$) and the second is when both the IGBTs are conducting ($\frac{1}{2} \leq D \leq 1$).

$$\Delta i_{in} = \begin{Bmatrix} \frac{V_o}{L}(1-2D)DT_s; 0 \leq D \leq \frac{1}{2} \\ \frac{V_o}{L}(2-2D)\left(D-\frac{1}{2}\right)T_s; \frac{1}{2} \leq D \leq 1 \end{Bmatrix} \quad (23)$$

The input current ripple is expressed as:

$$\Delta i_{in} = \frac{V_o}{L}(2-2D)\left(D-\frac{1}{2}\right)T_s \quad (24)$$

The overall voltage gain of the converter is defined by:

$$M = \frac{V_o}{V_{in}} \quad (25)$$

The input and output currents of the converter are expressed as:

$$i_{in} = i_o M \quad (26)$$

$$i_o = \frac{M}{Q} \quad (27)$$

where $Q = \frac{R_o}{Z_o}$ and characteristic impedance $Z_o = \sqrt{\frac{L_a}{C_a}}$.

$$i_{in} = \frac{M^2}{Q} \quad (28)$$

The output resistance R_o is selected by satisfying the following condition:

$$R_o \geq \frac{V_{in}}{(1-D)i_o} \quad (29)$$

The values of resonant elements L_a, C_a, L_b, and C_b are selected by taking the Q factor equal to 3 and characteristic impedance Z_o. The input inductance values of L_1 and L_2 are chosen by the following condition:

$$L \leq \frac{V_{in}D}{\Delta i_{pv} f_s} \quad (30)$$

The output filter capacitance C_o is taken from:

$$C_o = \frac{DV_o}{R_o \Delta V_o f_s} \quad (31)$$

The maximum values of the voltage stress of the IGBT and the current stress of input inductors are determined by the following expressions:

$$V_{igbt} = V_{in}\left(\frac{M^2}{Q}\right) \quad (32)$$

$$i_{Lmax} = \frac{V_{in}\left(\frac{M^2}{Q}\right)}{Z_o} \quad (33)$$

IV. SIMULATION ANALYSIS AND EXPERIMENTAL RESULTS

The PLECS software tool was used to design and simulate the proposed soft-switched IBC. The following values were used as simulation parameters: input voltage: 50 V, switching frequency: 40 kHz, output voltage: 320 V, inductors L_1, L_2 = 100 µH, resonant inductors L_a, L_b = 1.5 µH, resonant capacitors, C_a, C_b = 2 nF, and output capacitor C_o = 470 µF. Figure 6 shows the voltage and current waveforms of the S_1 and S_2 IGBTs. According to the waveforms obtained, the voltages of the IGBTs reach zero smoothly, therefore, the ZVS condition is achieved without any additional voltage and current stresses.

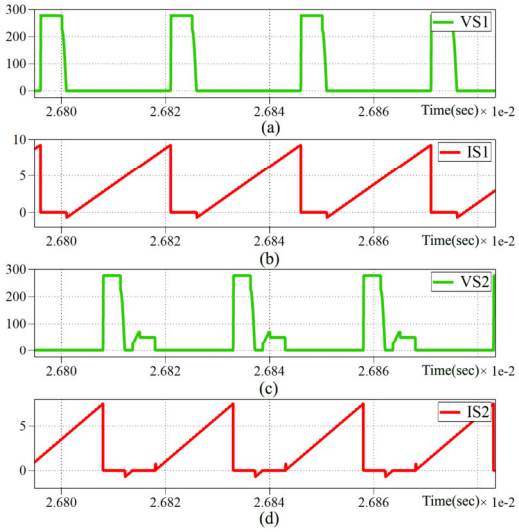

Fig. 6. Simulated waveforms: (a) V_{S1}, (b) i_{S1}, (c) V_{S2}, and (d) i_{S2}.

Figure 7 shows V_{Ca} and V_{Cb}. The waveforms obtained from the C_a and C_b resonant capacitors confirm that they are charged to the output voltage of 2/3 of V_o and discharge completely. Figure 8 shows the current through the resonant inductors L_a and L_b.

A 250 W prototype was built to validate the theoretical analysis. Table I shows the design parameters. The developed prototype was tested with a voltage of 50 V as input to get a 320 V output. The duty ratio was 0.85 and 0.6 for S_1 and S_2, respectively. The overall gain of the converter, while operating

at 50 V input voltage and obtaining an output voltage of 320 V, was approximately 6. The PWM signals were generated with the help of a Texas Instruments TMSF28335 module. The proposed converter operated at a switching frequency of 40 kHz. Infineon IHW25N120 IGBTs S_1 and S_2 were used, having 25 A maximum rated current with 1200 V maximum rated voltage. Two FKP2O11150 capacitors were connected in parallel to obtain a capacitance of 2 nF.

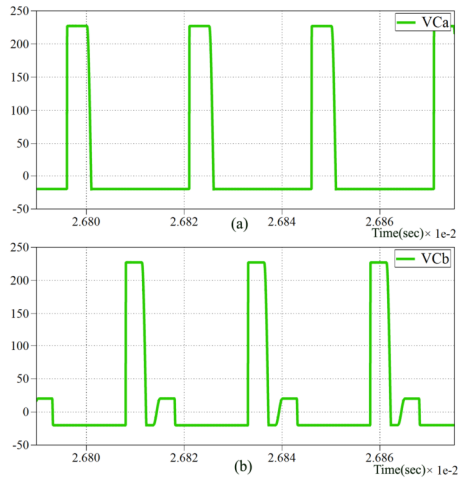

Fig. 7. Simulated waveforms of V_{Ca} and V_{Cb}.

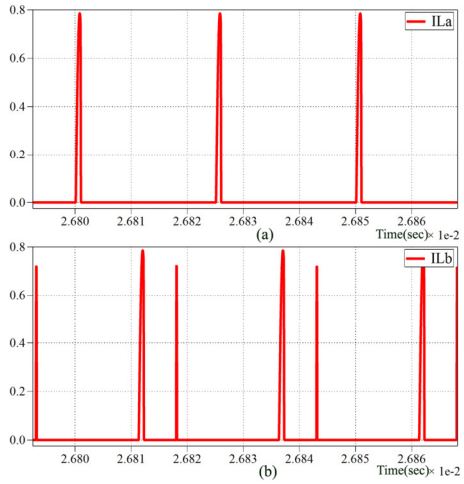

Fig. 8. Simulated waveforms of I_{La} and I_{Lb}.

TABLE I. LABORATORY PROTOTYPE PARAMETERS

Parameters	Symbol	Value
Input voltage	V_{in}	50 V
Output voltage	V_o	320 V
Switching frequency	f_{sw}	40 kHz
Output power	P_o	250 W
Inductors	L_1, L_2	100 µH
Resonant inductors	L_a, L_b	1.5 µH
Resonant capacitors	C_a, C_b	2 nF
IGBTs	S_1,S_2	IHW25N120
Diodes	D_1, D_2, D_a, D_b, D_c, D_d	C6D06065A

Figure 9 shows the collector-emitter voltage and collector currents of the S_1 and S_2 IGBTs. The proposed converter operates at a 50 V input voltage to produce a 320 V output voltage at a 400 Ω load resistance. The voltage stresses of the IGBTs are observed to be near 230 V, which is lower than the output voltage. The waveforms obtained validate the theoretical analysis, and the S_1 and S_2 IGBTs are turned on with the ZVS condition. When the converter operated at 30 V input voltage, it obtained 260 V output with the same duty ratios. Figure 10 shows the collector-emitter voltage and collector currents of the S_1 and S_2 IGBTs. The obtained waveforms demonstrate the ZVS condition.

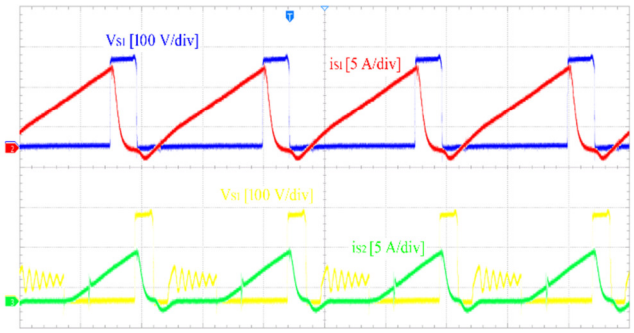

Fig. 9. Experimental waveforms for V_{in} = 50 V, V_o = 320 V. (top): V_{S1}: S_1 collector-emitter voltage, i_{S1}: collector current. (bottom): V_{S2}: S_2 collector-emitter voltage, i_{S2}: collector current (time scale: 10 µs/div).

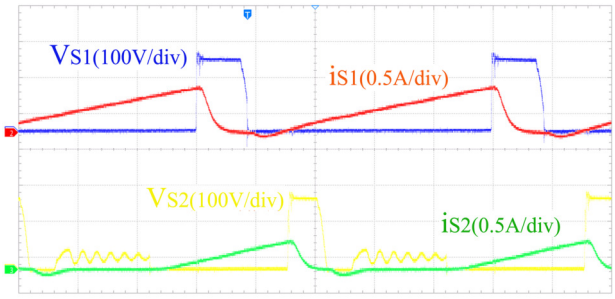

Fig. 10. Experimental waveforms for V_{in} = 30 V, V_o = 250 V. (top): V_{S1}: S_1 collector-emitter voltage, i_{S1}: collector current. (bottom): V_{S2}: S_2 collector-emitter voltage, i_{S2}: collector current (time scale: 5 µs/div).

Figure 11 shows the voltage waveforms across the C_a and C_b resonant capacitors. It can be seen that the capacitors are charged up to the output voltage of 240 V and discharge smoothly. Figure 12 depicts the current flowing through the L_a and L_b inductors. The maximum current flowing through the inductors is 0.8 A, which is the output current. Figure 13 shows the turn-on transients of the main IGBTs, S_1 and $S2$. Without current or voltage stresses and lower dv/dt rates, the soft-switching condition, ZVS turn on, is achieved, when the converter is operated at 100 W output power.

All IGBTs achieve ZVS turn-on conditions without any additional current or voltage stresses. The converter has an overall gain higher than that of existing converters. The aforementioned qualities are more advantageous than those of the prior IBCs. Table II shows the comparison between the

proposed soft-switched and existing IBCs. The proposed converter uses fewer auxiliary devices, experiences fewer turn-on losses, and achieves 97% efficiency at 250 W output power.

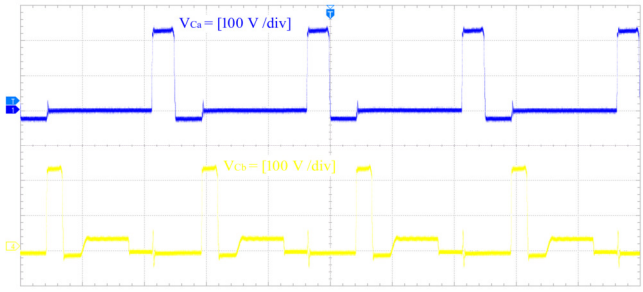

Fig. 11. Experimental waveforms. V_{ca}: C_a capacitor voltage (bottom), V_{cb}: C_b capacitor voltage (time scale: 10 µs/div).

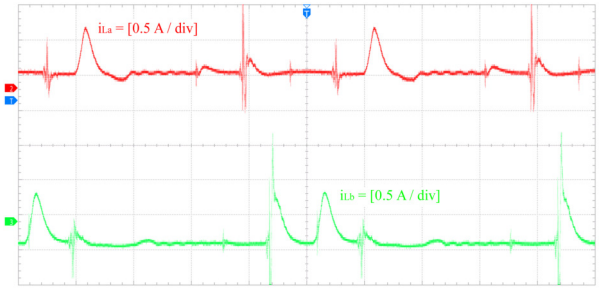

Fig. 12. Experimental waveforms. V_{ca}: C_a capacitor voltage (bottom), V_{cb}: C_b capacitor voltage (time scale: 10 µs/div).

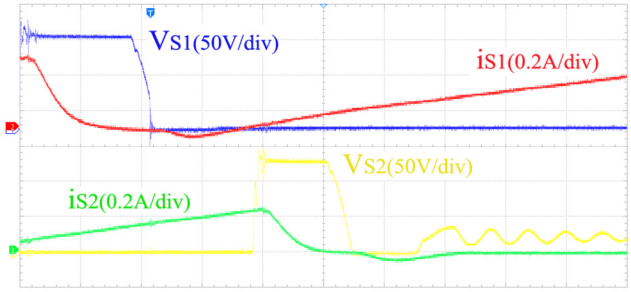

Fig. 13. Experimental waveforms. (top): V_{S1}: S_1 collector-emitter voltage, i_{S1}: Collector current, (bottom) V_{S2}: S_2 collector-emitter voltage, i_{S2}: collector current (time scale: 2 µs/div).

TABLE II. COMPARISON OF EXISTING CONVERTERS

	NS	ND	NL	NC	NRL	NRC	V_{in}	V_o	TDC
[12]	5	5	8	8	1	No	46	850	27
[14]	3	5	2	1	1	3	24	42	15
[16]	4	2	1, 1*	1	No	2	200	400	10
[17]	3	6	2*	5	No	1	48	400	17
[25]	2	6	2	1	2	2	200	400	17
Proposed converter	2	6	2	1	2	2	50	320	16

NS: number of switches, ND: number of diodes: NL: number of inductors: NC: number of capacitors: NRL: number of resonant inductors : NRC: number of resonant capacitors: *Coupled inductor, TDC: Total device count V_{in}: Input voltage, V_o: Output voltage

Figure 14 shows the efficiency curves. The efficiency measured at the output power of 100 W was 94.5%, at 150 W was 94.8%, at 200 W was 96.3%, and at 250 was 97%. When the converter operated at 250 W output power, the proposed IBC's maximum efficiency was 97%.

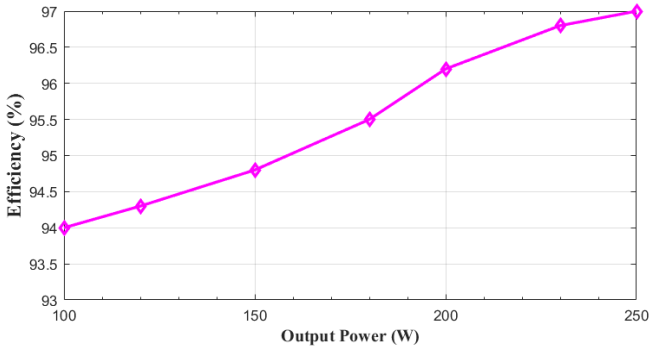

Fig. 14. Efficiency curve.

V. CONCLUSIONS

This study presented a novel two-phase IBC with passive lossless snubber cells, describing its design and operating concepts. There are no additional losses involved in achieving the ZVS condition. Using a 300 W laboratory prototype and a 50 V input voltage, the experimental investigations yielded a maximum output voltage of 320 V. The soft-switching ability of the proposed converter was tested up to the 250 W output power level. A passive lossless snubber provides ZVS turn-on of the IGBTs and plays an important role in achieving 97% efficiency. Compared to existing converters, the number of devices, including auxiliary switches, is reduced, thus reducing the overall cost. This proposed converter is suitable for medium- and high-power applications.

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AUTHOR PROFILES

Madhuchandra Popuri was born in Narasaraopet, India, in 1979. He received his B. Tech degree from JNTU Hyderabad in 2001 and M. Tech in Power and Industrial Drives from JNTUK, Kakinada, India, in 2013. His field of interest is Power Electronics. He has 17 years of teaching and research experience. He is currently a PhD Research Scholar in the School of Electrical Engineering, KIIT (Kalinga Institute of Industrial Technology) University, Bhubaneswar, India.

Veera Venkata Subrahmanya Kumar Bhajana received his B.E degree in Electronics and Communication Engineering from Sapthagiri College of Engineering, Dharmapuri, Tamilnadu, India (University of Madras) in 2000, his M.E from the P.S.N.A College of Engineering and Technology, Dindigul, Tamilnadu, India in 2005, and his PhD in Electrical Engineering from the Bharath University, Chennai, India in 2011. He has 17 years of teaching experience in various engineering institutes in India. He is previously associated as a post-doc researcher at the University of West Bohemia, Pilsen, Czech Republic from August 2013 to June 2015. He is currently working as an Associate Professor in the School of Electronics Engineering at KIIT University, Bhubaneswar, India since December 2011. He has presented papers in many reputed IEEE international conferences and has published many international journal (SCI) papers. His areas of interest include Power Electronics Engineering, Soft-Switching DC-DC converters, AC-AC converters, and multilevel converters.

M. K Maharana is currently an Associate Professor in the School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India. He has been working as an Associate Professor at the VIT University Vellore and as a software developer at GECE Hyderabad. He received his Ph.D in Electrical Engineering from the Indian Institute of Technology Madras, India in 2010. He received his M.Tech in power systems from NIT- Warangal (RECW) in 2001 and his B.S. from The Institution of Engineers, (India), Kolkata, in 1997. During his research he received the Corps of Electrical and Mechanical Engineers #39; Prize 2010-2011. He has more than 20 years of teaching and research experience. He has published several papers in international and national journals and has attained several national and international conferences. He is a reviewer for IEEE Access, IEEE Power and Energy, and Elsevier journals. His areas of research interest are computer modeling of power systems, energy management systems, battery energy storage and monitoring systems, and smart grid.

Pravat Biswal was born in Bhubaneswar, India. He received the B.Tech. degree in electrical engineering from the C.V. Raman College of Engineering at Bhubaneshwar, Odisha, India in 2008 and the M.Tech. degree from NIT Warangal. He is currently a Ph.D. Research Scholar and an Assistant Professor in the KIIT University, Bhubaneswar, India.

Bhargav Appasani received his Ph.D. degree from the Birla Institute of Technology, Mesra, India. He is currently an Assistant Professor at the School of Electronics Engineering, KIIT University, Bhubaneswar, India. He has

published more than 120 articles in international journals and conference proceedings, 6 book chapters, and 4 books. He also has a patent filed to his credit. He is an academic editor and reviewer in various esteemed journals. His research interests are smart grid, cyber-physical systems, 5G, vehicular networks, etc.

Oproescu Mihai was born in Piteşti, Arges County, Romania, in 1974. He obtained his B.S. (2003) and PhD (2011) in electronics and telecommunications from the University of Pitești. Currently, he is an associate professor at the National University of Science and Technology Politehnica of Bucharest, University Center Pitesti, Romania. Between 2016 and 2020 he was the Dean of the Faculty of Electronics, Communications and Computers, and currently he is the General Administrative Director of the National University of Science and Technology Politehnica of Bucharest, and a professor at the Faculty of Electronics, Communications and Computers. He is the chairman of the ECAI Conference and a member of the TCP Board of several international conferences or indexed journals. He is a guest editor in many international journals.

Nicu Bizon was born in Albesti de Muscel, Arges county, Romania, in 1961. He received the B.S. degree in electronic engineering from the University Polytechnic of Bucharest, Romania, in 1986, and the PhD degree in Automatic Systems and Control from the same university, in 1996. From 1996 to 1989, he worked in the hardware design with the Dacia Renault SA, Romania. He is currently a professor at the National University of Science and Technology Polytechnic Bucharest, Pitești University Centre, Romania. He has received two awards from the Romanian Academy, in 2013 and 2016. He is an editor of 17 books and more than 600 papers in scientific fields related to energy. His current research interests include power electronic converters, fuel cell and electric vehicles, renewable energy, energy storage systems, microgrids, and control and optimization of these systems.