Boosting WLAN Performance Using a Hybrid Network-on-Chip Routing Architecture with Predictive Congestion Avoidance

Malathi Naddunoori
School of ECE, REVA University, Bengaluru, Karnataka, India
n.malathiraj@gmail.com (corresponding author)

M. Devanathan
School of ECE, REVA University, Bengaluru, Karnataka, India
devanathan.m@reva.edu.in

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ABSTRACT

The growing needs for high-throughput and low-latency Wireless Local Area Networks (WLANs) have created the need for efficient and congestion-aware routing architectures. Traditional Network-on-Chip (NoC) architectures based solely on either packet switching or circuit switching are often subject to latency overhead, resource underutilization, and high power usage in dynamic traffic conditions. This paper presents a Hybrid NoC-based WLAN routing architecture that merges Static Switch Allocator (SSA), Parallel Virtual Switch Allocator (PVSA) and Lookup-Ahead Bypass Route Computation (LBRC). The suggested architecture is a synergistic approach of integrating deterministic routing and predictive congestion avoidance to enhance throughput, reliability, and hardware efficiency. The system was implemented on an Artix-7 FPGA and evaluated under realistic traffic conditions. The experimental results show 93% reduction in the number of Look-Up Tables (LUTs), a 33% reduction in total power consumption, and a 32% reduction in overall timing delay compared with the traditional NoC architecture. Further, the suggested system enables the doubling of bandwidth (100 Mb/s to 200 Mb/s), reduces hop count, improves Quality of Service (QoS) to 95%, and significantly reduces the Bit Error Rate (BER). Unlike current hybrid NoC models, the current design integrates predictive bypass routing that is dynamically configured in response to the dynamics of WLAN traffic to provide a scalable and hardware-efficient solution to next-generation and beyond 5G wireless networks.

Keywords-hybrid switching; virtual circuit switching; WLAN router design; power efficiency; dynamic routing flexibility; Static Switch Allocator (SSA)

I. INTRODUCTION

The last few years have been marked by an unprecedented rate of growth of Wireless Local Area Networks (WLANs) with the spread of mobile devices, the boom in the expansion of Internet of Things (IoT)-based environments, and the increased necessity to connect to high-speed networks in residential, commercial, and public networks [1]. The global WLAN market has gained significant momentum, which has supported the digitalization of smart cities and facilitated continuous connectivity of data-intensive applications. With the exponentially growing network traffic, the conventional WLAN routing processes are finding it difficult to cope with congestion, packet loss, varying throughput, and poor scalability, which are some of the challenges that have a major impact on the overall network functionality [2].

The latest systems such as healthcare monitoring systems, autonomous vehicles, industrial automation, and real-time collaborative systems require ultra-reliable and low-latency communication. Even the slightest inconveniences in the flow of data may result in severe failures such as failed medical reactions, unsafe driving, or factory shutdown [3]. Traditional static or semi-static routing table calculations cannot scale effectively in very dynamic and dense WLAN environments, particularly where thousands of IoT nodes are added to and removed from the network intermittently. This leads to router failures due to abrupt increases in traffic and consequently, to slow delivery of packets and underutilization of network resources [4].

Authors in [5] present an in-depth discussion of how 5G wireless technology can be used to develop smart home automation systems, especially focusing on low-latency communication, the possibility of connecting very large numbers of devices, and improved reliability. The paper is a systematic analysis of the roles of major 5G capabilities, including enhanced Mobile Broadband (eMBB), Ultra-Reliable

Low-Latency Communications (URLLC), and network slicing in the context of real-time control, seamless interoperability, and scalable integration of heterogeneous IoT devices in smart homes. The authors also present areas of application such as energy management, security surveillance, health-care monitoring, and intelligent appliances, in which they state that performance gains are ensured compared with previous wireless technologies. Although the review is quite successful in its ability to summarize current trends as well as viable applications, it also mentions unanswered issues surrounding security vulnerabilities, interoperability limitations, deployment expenses, and spectrum management. Altogether, the article is a valuable contribution to the topic of 5G-enabled smart homes as an application-level study; nevertheless, it is highly abstract and fails to cover architectural and routing-level optimization needs of large-scale and congestion-conscious network infrastructures.

Authors in [6] examine the role of interconnect topology and bandwidth availability in the performance of Distributed Shared Memory (DSM) systems. Their analysis shows that the efficiency of DSM is not only related to the mechanism of coherence or consistency but also to the network architecture and link capacities underlying DSM. These results highlight the fact that the problem of scalability in multi-node/multi-core systems is often due to communication patterns, localization of contention, and bandwidth–latency trade-offs, and thus provide the incentive to implement topology-conscious design and resource provisioning solutions.

Authors in [7] propose FARSI, a domain-specific System-on-Chip (SoC) design space exploration framework that is designed to manage the complexity of domain-specific designs. FARSI proposes a systematic search through architectural options to find a better trade-off between performance, power/energy, and area at the beginning of the design cycle when design changes are relatively cheap and formative. These frameworks are becoming more essential, as modern SoCs provide the ability to design using combinatorial design options; the Design Space Exploration (DSE) tools can also be used to convert application needs into a feasible architecture, and the time-to-design is also reduced.

Authors in [8] concentrate on 3D Network-on-Chip (NoC) architectures where vertical connections can be partially connected, hence enforcing non-uniform routing constraints. The approach that they have suggested, named AdEle+, is aimed at adaptive elevator selection, i.e. the efficient use of vertical traversal resources, taking into consideration congestion and energy. The aim of this strategy is to improve throughput and latency and to simultaneously reduce power consumption. The work is in line with the general trend: with 3D integration becoming the new reality, routing and resource selection policies will have to be adaptive to non-uniformities in space and dynamic traffic.

Authors in [4] offer an in-depth analysis of the needs and facilitating technologies for Quality-of-Service (QoS) provisioning of the Tactile Internet in the beyond-5G paradigm. The study singles out ultra-low latency, high reliability, and deterministic packet delivery as the main performance factors that underpin real-time applications of haptic communication, remote control, and immersive cyber-physical systems. The most important enablers such as edge computing, network slicing, intelligent scheduling, and cross-layer QoS management are discussed, with special attention to their ability to meet the strict delay and jitter requirements. In [9], the PaCHNOC is presented as a hybrid packet-circuit switching NoC design that is designed to support real-time parallel streams of data that have strict requirements on latency and reliability. In the design, circuit switched pathways are incorporated to ensure high throughput and predictability in communication as well as the use of packet switched paths to ensure flexibility due to dynamic traffic conditions. Both architectural elegance and sensible sharing of resources result in reduced congestion, lower latency constraints, and better throughput compared with traditional NoC routers that use packet switching. The paper therefore highlights the effectiveness of hybrid switching platforms in controlling inconsistent traffic patterns, thus offering a strong incentive to utilize hybrid NoC platforms in both latency-sensitive and congestion-prone networking platforms.

The next generation 6G communications are intended to support very low latency (below one millisecond), support very high density of devices, and facilitate smart network coordination. Although the radio layer improvements in 6G are aimed at spectrum efficiency and minimization of air-interface latency, intra-router congestion and routing delays remain a critical issue. The suggested Hybrid NoC architecture can be considered as a tool to fill the gap with the focus on the optimization of internal routing latency, predictive congestion avoidance, and enhanced hardware-level efficiency. Therefore, the suggested design is complementary to the developments of 6G and can be extended to dense IoT-enabled WLAN networks envisaged in future wireless systems. Despite significant progress having been made on adaptive and hybrid routing architectures of NoC, the existing solutions are either focused on the deterministic optimal packet-switching or adaptive, congestion-sensitive routing alone. Many of the existing literature do not consider the use of predictive bypass routing with deterministic allocation schemes that are explicitly designed to support the dynamics of WLAN traffic. Additionally, Artificial Intelligence (AI)-based routing mechanisms have overheads of runtime learning and increased hardware complexity, reducing their applicability to resource-constrained WLAN routers. The research gaps that were identified include:

- In hybrid NoC models, there are no predictive congestion avoidance mechanisms.
- Lack of routing optimizations to WLAN environments.
- High hardware costs of AI-based routing schemes.
- Lack of integration between deterministic and adaptive routing plans into a single model.

To address these drawbacks, this paper suggests a Hybrid NoC-based WLAN routing architecture that combines Static Switch Allocator (SSA), Parallel Virtual Switch Allocator (PVSA), and Lookup-Ahead Bypass Route Computation (LBRC). The significant contributions of the paper are:

- A hybrid structure that will incorporate deterministic and predictive paths.
- A 93% reduction in the use of Look-Up Tables (LUTs).
- A 33% reduction in total power consumption.
- A 32% reduction in end-to-end timing delay.
- Improved WLAN performance through doubling the bandwidth and reducing hop count.

II. SYSTEM ARCHITECTURE AND HYBRID ROUTING

The Hybrid NoC-based WLAN routing architecture presented incorporates three fundamental mechanisms, namely, SSA, PVSA, and LBRC, to build a robust, congestion-sensitive, and adaptive data transmission architecture [10]. The SSA offers deterministic switch allocation and low overhead allocation of switches in steady-state traffic conditions, whereas the PVSA offers parallel arbitration in several virtual channels, hence improving throughput in high contention environments. At the same time, LBRC allows early decision making in routing by precomputing the next hop paths, and this minimizes routing latency and allows avoidance of congested nodes. Combined, these mechanisms enable the WLAN system to be highly efficient in throughput, reduce latency between end-points, and provide message delivery reliability even in dynamic and fault-prone network situations [11]. Figure 1 illustrates the general structure of the proposed Hybrid NoC router, where all the routing, allocation, and switching elements are closely coupled into a single pipeline of communication.

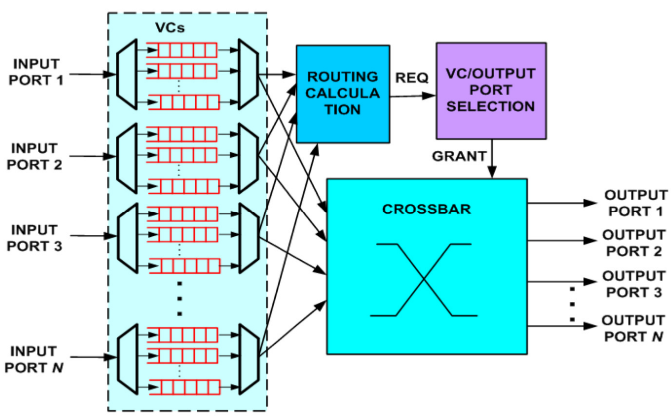

Fig. 1. Architecture of the proposed Hybrid NoC router.

The input unit receives the incoming WLAN information streams, and the packets are temporarily stored, after which a clock-controlled pipeline aligns the packets using registers [12]. The buffered packets are then passed through the SSA, the PVSA, and the LBRC stages in that order. In this process, the best routing and switching decisions are set gradually, followed by the packets being sent to the output unit [13]. This tight-coupled scalable architecture enables effective WLAN communications at a range of traffic loads, both at low-traffic and highly saturated conditions [14].

The first routing decision module in the architecture is the SSA. Figure 2 shows that SSA uses the packet header to decide which ports are used as inputs and outputs and then uses internal control structures, such as Next Routing Chip (NRC), Virtual Address (VA), Switch Table (ST), and Link Table (LT) to generate routing metadata. Based on these metadata, the SSA establishes deterministic and fixed routing paths according to the evaluation of crossbar availability, integrity of links, and path conflicts [15]. This deterministic allocation ensures that, in regular operating conditions of the network, the packets are routed over the most efficient and contention-free paths through the router, and hence limits latency and eliminates unnecessary contention [16].

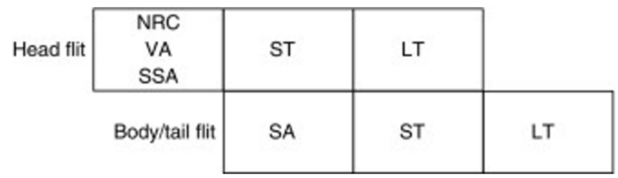

Fig. 2. SSA packet structure.

Some of the factors that make WLAN traffic patterns inherently dynamic include the mobility of nodes, changing traffic loads, and intermittent link availability [17]. To successfully overcome these issues, the proposed architecture uses the PVSA as a backup adaptive routing mechanism, as shown in Figure 3. Activation of the PVSA happens when the deterministic paths determined by the SSA experience congestion or link degradation, and thus dynamic rerouting via alternative virtual paths can be established [18].

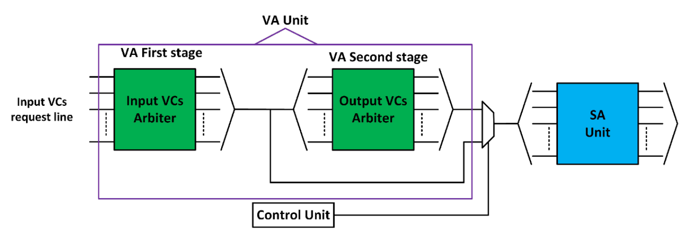

Fig. 3. PVSA operational diagram.

The PVSA uses a two-stage allocation scheme, which consists of Virtual Channel Allocation (VA) and Switch Allocation (SA). The two-layer system allows temporarily redirecting packets to circumvent overloaded or failed paths without stalling data transmission and maintaining data flow [19]. The PVSA effectively allocates traffic load and reduces contention by making use of parallel arbitration over a number of virtual channels, without interference on the main routing pipeline. The PVSA includes a virtual-channel-based switching that is combined with the flexibility of packets, adding a significant level of fault tolerance and congestion resilience. The design reduces latency spikes and ensures that throughput remains constant under unexpected WLAN conditions, and promotes network robustness and reliability as a whole [20].

In order to increase routing efficiency further, the suggested architecture applies the LBRC unit, as demonstrated in Figure

4. The LBRC constantly scans the state of the network and carries out predictive routing analysis to identify where potential hotspots of congestion can occur even before they result in stalled packets or link failures. It uses horizontal, vertical, and local routes bypass, along with specific bypass switches, to calculate alternative low-latency routes ahead of time [13]. The LBRC anticipates congestion and therefore proactively notifies the PVSA to enable bypass routing, therefore avoiding the delay of packets waiting until congestion is detected or failure occurs. This future-based routing policy is especially relevant for latency-conscious WLANs, where transient delays can be debilitating to QoS [16].

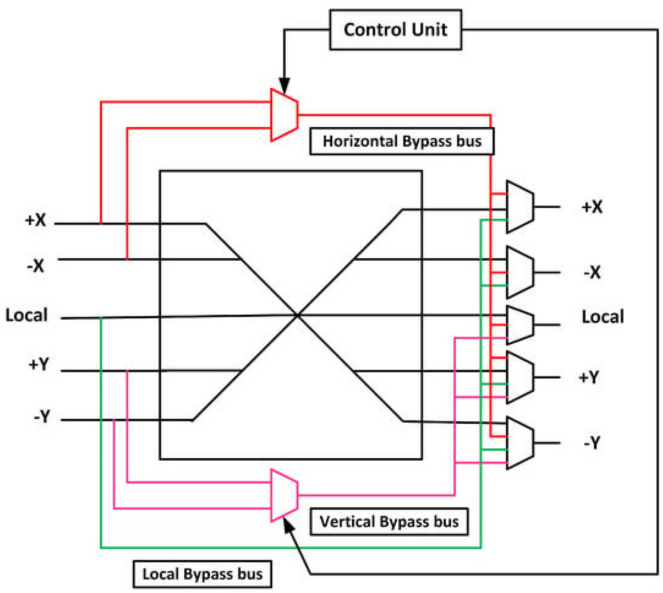

Fig. 4. LBRC operational diagram.

Altogether, the SSA provides the best deterministic paths in steady state, the PVSA provides dynamic flexibility in times of congestion or failure, and the LBRC provides predictive information for preemptive decisions of routing [21]. The close combination of these three elements can be defined as a Hybrid NoC routing methodology, which has remarkable advantages in enhancing data transmission efficiency, avoiding congestion, preventing packet loss, and improving the reliability of the entire WLAN system performance [22].

III. RESULTS AND DISCUSSION

The proposed Hybrid NoC architecture was implemented and evaluated using FPGA-based synthesis and simulation under controlled traffic scenarios. The simulation and implementation parameters used in this study are presented in Table I. This configuration ensures scalable evaluation under realistic WLAN traffic conditions.

The proposed Hybrid NoC architecture was developed and tested on an Artix-7 FPGA platform using Verilog and Xilinx Vivado. The outcomes reveal that the routing efficiency, resource usage, and timing performance are significantly better than current approaches based on NoC. Simulation was initially used to verify the functional behavior of the system, as depicted in Figure 5, where the results A′ and B′ are the expected outputs of the system at N = 32. This proves the accuracy of the interactions of SSA, PVSA, and LBRC in the suggested router.

TABLE I. SIMULATION AND IMPLEMENTATION PARAMETERS

Parameter	Configuration
Topology	4 × 4 mesh
Number of nodes	16
Processing elements (N)	32
FPGA platform	Xilinx Artix-7
Design tool	Vivado
Traffic pattern	Uniform + hotspot
Operating frequency	1 GHz

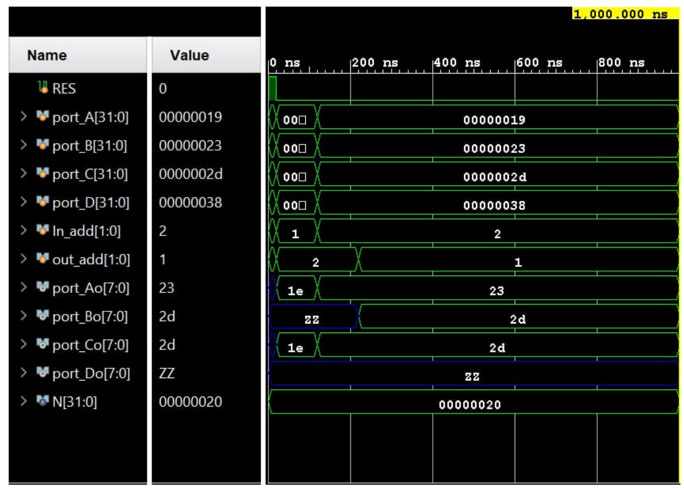

Fig. 5. Simulation results of the proposed NoC architecture for N = 32.

A comparative analysis of the area is provided in Table II and indicates significant improvements in LUT and I/O usage. The proposed approach lowers the LUT from 1,964 (Basic NoC) to only 135, which is an improvement of 93.1%. Likewise, the use of I/O decreases from 452 to 261, which is a 42% decrease. The proposed design provides the smallest hardware footprint among the considered methods, as shown in Table II. This is due to optimized resource sharing and the hybrid switching structure, which minimizes redundant routing circuitry.

TABLE II. AREA COMPARISON OF VARIOUS NOC METHODS

Metric	Basic NoC	MPSoC	NoCGuard	HSVLN	Proposed method
LUT	1,964	793	463	234	135
I/O	452	401	325	301	261

The power analysis, as summarized in Table III, indicates significant improvement in all dynamic power aspects. The overall power consumption is reduced by 33% in the proposed design compared with 5.827 W (Basic NoC). Figure 6 provides a visual breakdown of static and dynamic power values. The reduction results from efficient virtual switching, reduced logic toggling, and minimized path redundancy through LBRC-assisted bypassing.

TABLE III. POWER COMPARISON OF VARIOUS NOC METHODS

Component	Basic NoC (W)	MPSoC (W)	NoCGuard (W)	HSVLN (W)	Proposed method (W)
Signal	4.528	4.825	4.125	3.925	3.019
Logic	0.419	0.464	0.383	0.377	0.290
I/O	0.712	0.654	0.621	0.589	0.475
Dynamic	5.659	5.943	5.129	4.891	3.785
Static	0.168	0.147	0.155	0.137	0.117
Total	5.827	6.090	5.284	5.028	3.902

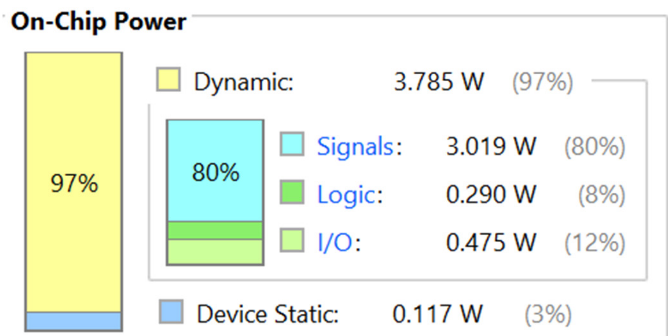

Fig. 6. Power consumption of the proposed NoC for N = 32.

Timing performance, detailed in Table IV, indicates major improvements in setup and hold delays. Total delay decreases from 29.089 ns (Basic NoC) to 19.665 ns—a 32.4% improvement—primarily due to streamlined routing stages and bypass logic that reduces long-path congestion.

TABLE IV. DELAY COMPARISON OF VARIOUS NOC METHODS

Component	Basic NoC (ns)	MPSoC (ns)	NoCGuard (ns)	HSVLN (ns)	Proposed method (ns)
Setup logic delay	5.679	6.081	5.271	4.865	3.982
Setup net delay	21.046	20.213	19.569	18.768	15.683
Total setup delay	26.725	26.294	24.840	23.633	19.665
Hold logic delay	0.637	0.578	0.552	0.498	0.421
Hold net delay	1.070	1.092	1.036	0.997	0.874
Total hold delay	1.707	1.670	1.588	1.495	1.295
Total delay	29.089	28.288	26.628	25.128	19.665

The combination of SSA's deterministic routing and LBRC's predictive bypassing significantly lowers the critical path length, improving overall data throughput. The introduction of Hybrid NoC mechanisms directly enhances WLAN routing characteristics. The proposed method doubles bandwidth (100 Mb/s → 200 Mb/s), reduces hop count (5 → 3), and improves QoS (85% → 95%). The reduction in Bit Error Rate (BER) to 3×10^{-9} indicates high link reliability. These improvements validate the feasibility of deploying NoC-based routing in real-world WLAN systems requiring low latency and congestion-free communication.

IV. WLAN PERFORMANCE ANALYSIS

The feasibility of the proposed Hybrid NoC-based WLAN routing architecture was assessed using a series of important communication metrics in order to ascertain its applicability to real-world WLAN conditions. These measures are bandwidth, number of hops, frequency of operation, path length, QoS, BER, and overall communication efficiency. A comparison with conventional NoC-based WLAN routing techniques shows significant enhancements due to the integration of SSA, PVSA, and LBRC mechanisms.

Among the most notable improvements is bandwidth, where the proposed method doubles the supported data rate from 100 Mb/s to 200 Mb/s. This improvement is attributed to the optimization of routing paths and more efficient congestion management through dynamic allocation of virtual paths and predictive bypassing. The architecture reduces contention and enhances packet flow, resulting in increased data throughput, which is crucial in high-performance WLAN applications like video streaming, online gaming, telemedicine, and industrial control. The hop count, representing the number of intermediate routers a packet traverses, is reduced from 5 to 3 in the proposed system.

The operating frequency is increased from 500 MHz to 1 GHz. This increase can be attributed to hybrid routing strategy, which reduces the critical path length and improves timing performance. The path length is also reduced from 10 units to 6 units. Shorter path lengths reduce latency and decrease the likelihood of encountering congested or faulty links. This improvement results from the deterministic selection of SSA and the ability of PVSA to construct temporary virtual paths when the primary path is overloaded or unavailable.

QoS increases from 85% to 95%. This improvement demonstrates the capability of the proposed method to deliver consistent and reliable communication under dynamic traffic loads. The direct advantages of QoS are lower packet loss, reduced jitter, and faster recovery from congestion events, all provided by the hybrid NoC mechanisms. The BER decreases significantly, from 10^{-6} to 3×10^{-9}. This three-order-of-magnitude improvement indicates higher signal reliability and reduced error sensitivity.

The hybrid switching strategy ensures fewer packet collisions and cleaner routing paths, reducing the likelihood of data corruption. Overall, compared to traditional systems, the proposed architecture achieves higher bandwidth, lower latency, improved reliability, and enhanced routing performance.

To clearly demonstrate the effectiveness of the proposed Hybrid NoC routing architecture, a consolidated comparison with representative NoC designs is presented in Table V. The results confirm substantial improvements in hardware efficiency and latency reduction compared to conventional and hybrid NoC models.

TABLE V. CONSOLIDATED COMPARISON OF NOC METHODS

Metric	Basic NoC	HSVLN	Proposed method
LUT	1,964	234	135
Total power (W)	5.827	5.028	3.902
Total delay (ns)	29.089	25.128	19.665
Bandwidth (Mb/s)	100	150	200

V. CONCLUSION

The proposed Hybrid Network-on-Chip (NoC)-based Wireless Local Area Network (WLAN) routing architecture demonstrates a significant improvement in congestion prevention, routing efficiency, and overall communication performance. To provide a robust, responsive, and fault-tolerant routing system, it incorporates Static Switch Allocator (SSA), Parallel Virtual Switch Allocator (PVSA), and Lookup-Ahead Bypass Route Computation (LBRC) to address the limitations of traditional routing in WLAN-integrated systems. SSA ensures deterministic path selection, whereas PVSA enables dynamic virtual path formation to handle congestion and fault recovery, and LBRC provides predictive bypassing of potential bottlenecks. The integration of these mechanisms results in a seamless hybrid switching environment, which minimizes latency, maximizes throughput, and reduces packet loss.

The results demonstrate that key performance metrics are significantly improved. The architecture provides a 93% reduction in Look-Up Table (LUT) usage, a 33% reduction in total power consumption, and over a 32% reduction in timing delay compared with conventional NoC-based approaches. Although the presented Hybrid NoC architecture has been tested at both FPGA and architectural levels, future work will focus on real-world WLAN implementation and large-scale deployment within Software-Defined Networking (SDN) environments. Its design can also be generalized to Software-Defined Data Centers (SDDCs) as well as edge-computing infrastructure, where congestion-aware routing is critical. Further studies will focus on real-time WLAN implementation and integration with programmable network controllers.

DECLARATION OF COMPETING INTERESTS

The authors declare that they have no known competing financial interests or personal relationships.

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Not applicable to this work.

DATA AVAILABILITY

The datasets and design files of this study are available from the authors upon reasonable request.

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