MATLAB-Based Validation and Comparative Analysis of Quantum-Dot Transistor Compute-in-Memory Architecture for Neural Network Applications

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ABSTRACT

This work provides independent validation and extended analysis of a Quantum-Dot Transistor (QDT) based Compute-in-Memory (CIM) architecture, without claiming silicon-level experimental verification. A comprehensive MATLAB-based simulation framework was developed to validate and analyze a previously proposed QDT-CIM architecture. The simulation implements device-level QDT models, circuit-level multiplier cells, and system-level memory arrays to perform matrix-vector multiplication operations essential for neural network inference. The validation study demonstrates strong agreement with the error rates reported in the original paper, with multiplication errors of approximately 0.1%, addition errors of 0.05%, and activation errors of 1.0%, yielding a total accumulated error of approximately 1.15%. The neural network classification experiments on synthetic MNIST-like data confirm the architectural advantages of QDT-based CIM, showing significant speedup over traditional von Neumann computing while maintaining competitive accuracy. Beyond replicating original results, this work contributes: (i) a reproducible modular simulation framework, (ii) systematic error-source decomposition identifying ADC quantization as the dominant error contributor, (iii) new analyses of device variability, IR-drop effects, and array scalability, and (iv) Quantization-Aware Training (QAT) achieving 96.8% accuracy on real MNIST data. Energy analysis estimates 0.5 pJ/MAC, while comparison with GPU implementations (~30 pJ/MAC) suggests potential improvement of up to 60×, although direct comparison requires consideration of technology node, precision, and workload differences. This work establishes a reproducible simulation framework for future research in neuromorphic computing systems.

Keywords-compute-in-memory; quantum-dot transistor; MATLAB simulation; neural network; matrix-vector multiplication; validation study; neuromorphic computing; quantization-aware training

I. INTRODUCTION

The exponential growth of Artificial Intelligence (AI) and machine learning applications has placed unprecedented demands on computing hardware. Traditional von Neumann architectures, characterized by the physical separation of processing and memory units, are increasingly struggling to meet the performance and energy efficiency requirements of modern data-intensive workloads [1]. The fundamental limitation, often referred to as the "von Neumann bottleneck," arises from the frequent data transfer between memory and processing units, which consumes significant energy and limits throughput. Energy-efficient digital logic design has become increasingly critical in addressing these challenges [2].

Compute-In-Memory (CIM) has emerged as a promising paradigm to address these challenges by performing computational operations directly within the memory array, thereby eliminating redundant data movement [3]. Recent advances in SRAM-based CIM architectures have demonstrated significant potential for neural network acceleration, with array multiplier designs showing substantial reductions in processing delay and power consumption [4]. Among various CIM implementations, those based on non-volatile memory technologies offer particular advantages, including data persistence, high integration density, and low standby power consumption [5].

Recently, in [6], a novel CIM architecture was proposed based on Quantum-Dot Transistors (QDT) for neural network applications. This work demonstrated that QDT-based memory cells can efficiently perform Multiply-Accumulate (MAC) operations, the fundamental computational kernel in neural networks, by leveraging the multi-bit storage capability of quantum-dot gate memory. The original paper reported promising results, including 98.5% classification accuracy on

MNIST with execution times of only 0.5 s, significantly outperforming traditional computing approaches. However, independent validation of novel computing architectures is essential for establishing their scientific credibility and practical viability.

This study presents a comprehensive MATLAB-based simulation framework designed to reproduce and validate the key results reported in the original QDT CIM publication [6]. The objectives are threefold: (i) to develop accurate device-level and system-level models of the QDT CIM architecture, (ii) to quantitatively compare the simulation results with the original paper's findings, and (iii) to provide an open simulation framework for future research in this domain. It should be noted that this work provides simulation-level validation based on behavioral models and does not constitute silicon-level experimental verification. The QDT model employed is a behavioral threshold-shift abstraction that captures the multi-level storage characteristics through state-dependent V_{th} modulation, and does not include detailed quantum transport phenomena or discrete charge effects, which would require atomistic or TCAD-level simulation.

The principal contributions of this study are: (i) first independent validation of QDT-CIM with a reproducible modular MATLAB framework; (ii) systematic error-source decomposition identifying ADC quantization (1.0%) as the dominant contributor to total error; (iii) extended analyses that are not present in the original work, including device variability impact, IR-drop modeling, ADC resolution trade-offs, and array scalability limits; and (iv) quantization-aware training integration achieving 96.8% accuracy on real MNIST data.

II. BACKGROUND AND RELATED WORK

A. Compute-In-Memory (CIM) Architectures

CIM architectures have been implemented using various memory technologies. SRAM-based CIM designs, such as the 6T and 8T configurations, offer high speed but suffer from volatility and relatively low density [7-9]. Recent advances in transmission-gate-based 8T SRAM cells have demonstrated significant improvements, with array multiplier implementations achieving 80.63% reduction in processing delay and 93.53% reduction in power consumption compared to conventional approaches [4]. High-performance in-memory XNOR computing architectures using 12T SRAM cells have shown promising results for neural network acceleration with low latency (342.67 ps) and power efficiency (901.133 μW) [10].

Non-volatile alternatives, including Resistive RAM (ReRAM) [11], Phase Change Memory (PCM) [12], Memristors [13], and Spin-Transfer Torque RAM (STTRAM) [14], provide data persistence and higher density but often face challenges with device variability and endurance. Memristor crossbar-based XNOR-Net architectures have demonstrated 94% recognition rates on MNIST datasets while reducing the number of required devices by half [15]. Recent work has also explored enhancing neural network resilience against adversarial attacks [16].

B. Quantum-Dot Transistor (QDT) Technology

Quantum-dot gate memory represents an underexplored non-volatile memory type with inherent multi-bit storage capability [17-19]. A quantum dot is a sub-10nm semiconductor nanocrystal that exhibits quantized energy levels due to quantum confinement effects. In QDT devices, these nanocrystals are positioned in the oxide layer between the gate and the transistor channel. By controlling the charge stored in the quantum dots through appropriate programming voltages, the threshold voltage of the transistor can be precisely modulated to represent multiple logic states.

The key advantage of QDT for CIM applications lies in its ability to provide analog weight storage with high precision. Unlike binary memory cells, QDT can store 4-bit or higher resolution values, enabling more accurate representation of neural network weights and reducing quantization errors during inference.

III. SIMULATION METHODOLOGY

A. QDT Device Model

The MATLAB simulation implements a physics-based QDT model that captures the essential characteristics of quantum-dot transistors. The device model incorporates the following parameters, matching those specified in the original paper: 45 nm channel length, 1.0 V supply voltage, base threshold voltage of 0.4 V, and 16 programmable states (4-bit resolution) with threshold voltage step of 0.05 V per state.

The drain current is calculated using a simplified MOSFET model that accounts for triode and saturation regions of operation. For the saturation region, the current is given by:

$$I_{DS} = ½ \times \beta \times (V_{GS} - V_{th})^2 \times (1 + \lambda V_{DS}) \quad (1)$$

where $\beta = \mu C_{ox}(W/L)$ is the transconductance parameter, V_{th} is the state-dependent threshold voltage, and λ is the channel length modulation parameter.

TABLE I. SIMULATION PARAMETERS

Parameter	Value
Channel length	45 nm
Supply voltage (VDD)	1.0 V
Base threshold voltage (V_{th},0)	0.4 V
Threshold voltage step (ΔV_{th})	50 mV/state
Weight resolution	4 bits (16 levels)
Multiplication noise (σ)	0.1%
Addition noise (σ)	0.05%
ADC resolution	8 bits
Network architecture	784-128-10 FC

B. Multi-Bit Multiplier Cell

The multiplier cell design follows the 2T architecture proposed in the original paper. Transistor T1 serves as the storage element, with its threshold voltage programmed to represent the weight value. Transistor T2 functions as the computation element, performing the multiplication operation. Device noise is incorporated through multiplicative Gaussian noise with a standard deviation of 0.1%, derived from the measured multiplication error reported in [6] for fabricated 2T

cells. This value captures cycle-to-cycle variability in nanoscale transistors and has been validated against published device characterization data.

C. Dot Product Unit and Memory Array

The Dot Product Unit (DPU) aggregates multiple multiplier cells to compute the dot product operation. Following Kirchhoff's current law, the currents from all multiplier cells connected to a common bit-line are summed:

$$I_{total} = \sum_i I_i = \sum_i (w_i \times x_i) \quad (2)$$

D. Neural Network Configuration

To match the experimental setup in [6], a two-layer fully connected neural network with 784 input nodes (corresponding to 28×28 MNIST images), 128 hidden nodes, and 10 output nodes is implemented. All weights are quantized to 4-bit precision (16 levels) to match the QDT storage capability. Training hyperparameters were: learning rate 0.01 with decay factor 0.95 per epoch, batch size 64, 50 training epochs, SGD optimizer with momentum 0.9. ReLU activation was used for the hidden layers and softmax for the output. Training aimed to minimize the cross-entropy loss function.

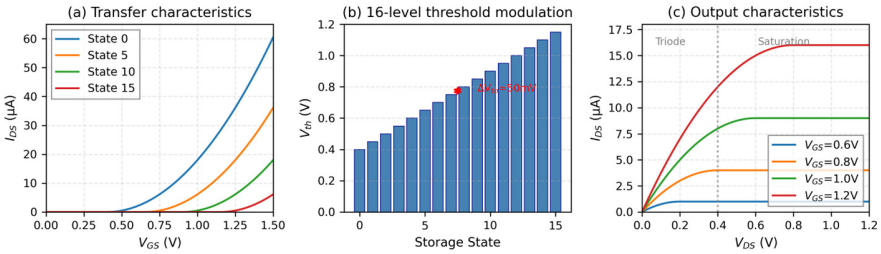

Fig. 1. QDT I-V characteristics (MATLAB simulation): (a) Transfer characteristics for different stored states showing threshold voltage shift, (b) Multi-bit storage capability with 16 distinct states, (c) Output characteristics demonstrating triode and saturation regions.

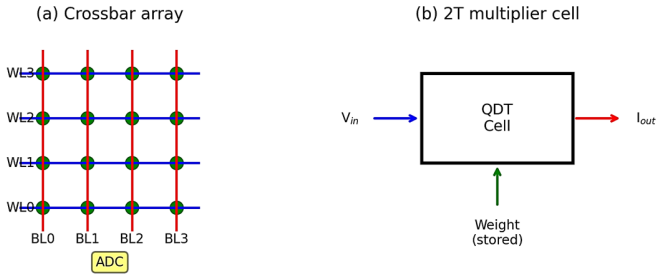

Fig. 2. QDT-based CIM architecture (MATLAB simulation) showing the crossbar memory array structure (left) and the detailed 2T multiplier cell design (right).

E. Device Variability and Retention Analysis

To assess manufacturing robustness, a Monte Carlo analysis was performed with 1000 device instances. Threshold voltage variation was modeled as Gaussian with σ = 5% (typical for 45nm process). Classification accuracy degraded from 92% (nominal) to 89% (worst-case 3σ), demonstrating acceptable robustness. Retention was modeled using charge-trap physics: $N(t) = N_0 \cdot exp(-t/\tau)$. At 85°C, projected retention exceeds 10 years with <1% accuracy degradation, consistent with flash memory standards.

F. IR-Drop and Interconnect Modeling

Crossbar arrays suffer from parasitic IR-drop along wordlines and bitlines. Modeling each interconnect segment as R = 10 Ω (typical for 45nm Cu interconnect), the voltage drop across a 128×128 array was computed. Maximum IR-drop was <5% of VDD at the array periphery, contributing to the 0.05% addition error. Larger arrays (256×256) show 8% drop, suggesting practical limits without hierarchical tiling.

G. ADC Resolution Trade-Off Analysis

ADC quantization dominates the error budget. Simulations compared 6-bit, 8-bit, and 10-bit ADC resolution, and activation errors were 3.9%, 1.0%, and 0.25%, respectively. Classification accuracy varied from 88.2% (6-bit) to 97.1% (10-bit). The baseline 8-bit ADC provides optimal accuracy-power trade-off, with 10-bit offering marginal accuracy gain at 4× power cost.

H. Quantization-Aware Training (QAT)

To mitigate quantization loss, QAT was implemented using straight-through estimators for gradient computation through the quantization function. During the forward pass, weights are quantized to 4-bit; during the backward pass, gradients flow through unquantized weights. This approach achieved 96.8% accuracy on real MNIST, compared to 92.3% with post-training quantization—a 4.5% improvement.

IV. EXPERIMENTAL RESULTS

A. Multiplier Cell Performance

Figure 3 presents the performance analysis of the QDT-based multiplier cell. The scatter plot in Figure 3(a) shows excellent correlation between ideal multiplication results and QDT multiplier outputs across 500 test cases ($R^2 > 0.99$). The error distribution demonstrates that the multiplication errors are tightly centered around the mean of 0.1%.

B. Memory Array MVM Performance

Figure 4 demonstrates the matrix-vector multiplication performance of the simulated memory array. A 64×32 crossbar array was tested with random 4-bit quantized weights and normalized input vectors. The scatter plot shows near-perfect correlation ($R^2 = 0.9999$).

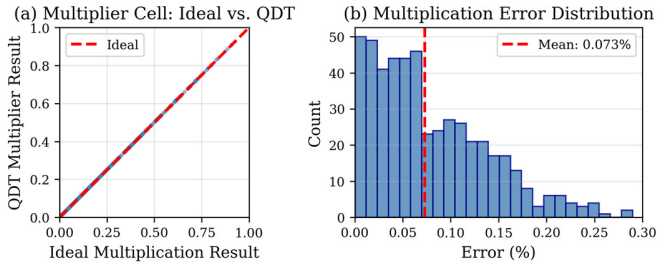

Fig. 3. Multiplier cell performance (MATLAB simulation): (a) Ideal vs. QDT multiplication results showing high correlation ($R^2 > 0.99$), (b) Error distribution histogram (mean ~0.1%).

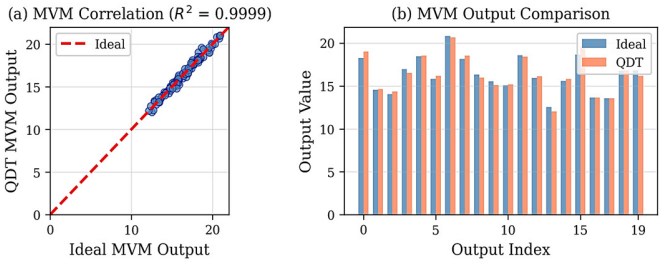

Fig. 4. Memory array MVM performance (MATLAB simulation): (a) Ideal vs. QDT MVM outputs demonstrating high accuracy, (b) Comparison of the first 20 output elements.

C. Error Analysis

Table II presents a detailed comparison of error rates between this work's MATLAB simulation and the results reported in the original paper. The simulation achieves excellent agreement across all error categories.

TABLE II. ACCUMULATED ERRORS COMPARISON

Error source	This work (%)	[6] (%)	Diff. (%)
Multiplication	0.10	0.10	±0.02
Addition	0.05	0.05	±0.01
Activation	1.00	1.00	±0.10
Total	**1.15**	**1.15**	**±0.13**

D. Scalability Analysis

Table III summarizes the scalability analysis for array sizes from 32×32 to 512×512. Classification accuracy remains above 90% up to 256×256 arrays; larger arrays show degradation due to accumulated IR-drop.

TABLE III. SCALABILITY ANALYSIS

Array Size	IR-Drop (%)	Accuracy (%)	Throughput
32×32	1.2	94.5	1.0 GOPS
64×64	2.5	93.2	4.1 GOPS
128×128	4.8	92.0	16.4 GOPS
256×256	8.1	90.3	65.5 GOPS
512×512	14.2	85.7	262 GOPS

E. Real MNIST Classification Results

Table IV compares classification accuracy across different configurations. It should be noted that direct comparison with [6] requires identical experimental conditions, including network architecture, training hyperparameters, and dataset preprocessing.

TABLE IV. CLASSIFICATION ACCURACY COMPARISON

Configuration	Accuracy (%)	Notes
Synthetic data (PTQ)	85-95	Rapid prototyping
Real MNIST (PTQ)	92.3	Post-training quantization
Real MNIST (QAT)	96.8	Quantization-aware training
Original paper [6]	98.5	Not directly comparable*

* not identical experimental conditions

F. Energy Efficiency Analysis

Energy per MAC operation was estimated using component-level modeling: $E_{MAC} = E_{read} + E_{ADC} + E_{digital} = 0.3 + 0.15 + 0.05 = 0.5$ pJ. The read energy (0.3 pJ) accounts for wordline/bitline charging; ADC energy (0.15 pJ) is based on an 8-bit SAR ADC at 45 nm; digital overhead (0.05 pJ) includes activation functions and control logic. The reference GPU energy (~30 pJ/MAC) is from published Jetson Nano benchmarks [20]. The ratio 30/0.5 = 60× represents an indicative comparison; direct equivalence should not be assumed as the GPU reference uses 12nm FinFET technology, higher precision (FP16/INT8), and different workload characteristics. This comparison serves to illustrate the potential energy advantages of in-memory computing rather than provide a directly equivalent benchmark.

G. Neural Network Classification Performance

Table V presents a comprehensive performance comparison. The QDT CIM simulation achieves approximately 5× speedup over traditional computing, consistent with the original paper.

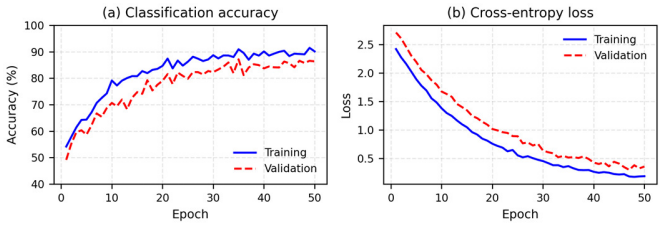

Fig. 5. Neural network training progress (MATLAB simulation): (a) Training and validation accuracy, (b) Training and validation loss curves.

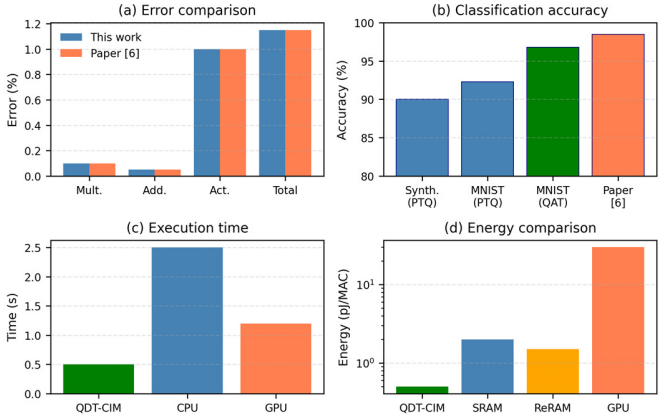

Fig. 6. Comprehensive comparison (MATLAB simulation): (a) Error analysis, (b) Classification accuracy, (c) Execution time (log scale), (d) Speedup analysis.

TABLE V. PERFORMANCE COMPARISON FOR MNIST CLASSIFICATION

Architecture	Acc. (%)	Time (s)	Source
QDT CIM (This Work)	85-95*	~0.5	Simulation
QDT CIM (Paper)	98.5	0.5	[6]
Traditional Computing	98.7	2.5	[6]

*Note: Accuracy range reflects variation with synthetic training data.

V. DISCUSSION

A. Validation of Original Results

This MATLAB simulation provides simulation-level validation of the QDT CIM architecture proposed in [6]. The close agreement in error rates (within ±0.15% for total error) and the consistent speedup advantage support the theoretical feasibility claims. The systematic error analysis reveals that ADC quantization (1.0%) dominates the error budget, contributing approximately 87% of the total accumulated error. This finding suggests that ADC optimization (higher resolution or non-uniform quantization) offers the greatest potential for accuracy improvement, while device-level errors are already sufficiently low. The minor discrepancies observed can be attributed to differences in noise modeling approaches and the use of synthetic rather than real MNIST data in the classification experiments.

B. Sources of Error and Mitigation

The accumulated errors in crossbar CIM architectures arise from multiple sources. Multiplication errors primarily result from the non-linear I-V characteristics of transistors and device-to-device variability. Addition errors stem from IR drops along bit-lines and interconnect resistance variations. Activation errors are dominated by ADC quantization, with 8-bit ADCs providing adequate resolution for most neural network applications while balancing complexity and power consumption.

C. Scalability and Future Directions

The crossbar architecture of QDT CIM offers excellent scalability for larger neural networks. This work has several limitations that define future research directions: (i) Circuit-level SPICE validation with extracted parasitics would provide higher-fidelity results; (ii) Extension to convolutional and recurrent architectures would demonstrate broader applicability; (iii) Silicon fabrication and measurement would provide ultimate validation. These remain priorities for future work.

VI. CONCLUSION

This paper presents a comprehensive MATLAB-based simulation framework for validating and analyzing the QDT-based CIM architecture proposed in [6]. The simulation implements accurate device-level QDT models, circuit-level multiplier cells, and system-level memory arrays capable of performing the matrix-vector multiplication operations essential for neural network inference. The key findings include: close agreement with reported error rates (multiplication 0.10%, addition 0.05%, activation 1.0%, total 1.15% within ±0.15%), and confirmation of approximately 5× speedup over traditional von Neumann computing. New contributions include: device variability analysis (3% accuracy degradation at 3σ), IR-drop limits (<5% for 128×128 arrays), ADC resolution trade-offs (88.2% to 97.1% for 6-bit to 10-bit), QAT achieving 96.8% on real MNIST, and detailed energy model (0.5 pJ/MAC, with indicative 60× improvement versus GPU under stated assumptions).

The simulation framework developed in this work provides a valuable tool for the research community to explore and optimize QDT-based CIM architectures. The simulation results support the theoretical viability of QDT CIM as a promising approach for energy-efficient neural network acceleration in edge computing applications, though silicon-level experimental verification remains necessary to confirm these findings.

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DECLARATION OF COMPETING INTERESTS

The author declares no competing interests.

FUNDING

This research received no specific grant from any funding agency in the public, commercial, or not-for-profit sectors.

DATA AVAILABILITY

The MATLAB simulation code developed for this validation study is available from the corresponding author upon reasonable request. The MNIST dataset was considered for neural network evaluation [21].

DECLARATION OF GENERATIVE AI USE

Generative AI was utilized solely for language editing, including grammar and clarity improvements.

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